IN THE CLAIMS:

What we claim as our invention is:

1. A mask layer overlaying a low k dielectric material deposited over an underlying metal layer of an integrated circuit device, for use in the construction of an interconnect structure of the integrated circuit device, said mask layer comprising:

(a) a passivation mask film deposited on the low-k dielectric material;

(b) a barrier mask film deposited over the passivaton mask film; and,

(c) a metallic mask film deposited over the barrier mask film.

2. The mask layer of claim 1 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

3. The mask layer of claim 1 wherein said barrier mask film comprises silicon nitride.

4. The mask layer of claim 1 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy.

5. The mask layer of claim 4 wherein said refractory metal is chosen from a group of refractory metals comprising titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refactory metal alloys comprising titanium nitride and tantalum nitride.

6. A method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material deposited over an underlying metal layer, comprising the steps of:

(a) forming a passivation mask film over the low-k dielectric material;

(b) forming a barrier mask film over the passivation mask film;

(c) forming a metallic mask film over the barrier mask film, and said passivation barrier and metallic mask films forming a mask layer overlaying said low-k dielectric material;

(d) etching a trench within the low-k dielectric material to a predetermined depth of the low-k dielectric material; and,

(e) etching a via through the low-k dielectric material to the underlying metal layer.

7. The method of claim 6 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

8. The method of claim 8 wherein said barrier mask film comprises silicon nitride.

9. The method of claim 8 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy

10. The method of claim 9 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.

11. The method of claim 6 further including the step of forming a photoresist layer over the metallic mask film, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film and the barrier mask film to the passivation mask film.

12. The method of claim 6 further including the step of forming a photoresist layer over the low-k dielectric material, and patterning a via feature in the photoresist layer.

13. The method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material deposited over an underlying metal layer, and a mask layer deposited on the low-k dielectric material, and said mask layer having a desired etch selectivity with respect to the low-k dielectric material, the method comprising the step of forming a metallic film as part of the mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer.

14. The method of claim 13 wherein said metallic film comprises a refractory metal or a refractory metal alloy.

15. The method of claim 14 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten and said refractory metal alloy is chosen from the group of refractory metal alloys including titanium nitride or tantalum nitride.

16. The method of claim 13 furthering including the steps of forming a passivation mask film over the dielectric material, forming a barrier mask film over the passivation mask film and said metallic film is formed over the barrier mask film.

17. The method of claim 15 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

18. The method of claim 15 wherein said barrier mask film comprises silicon nitride.

19. The method of claim 13 further including the steps of etching a trench within the low-k dielectric material to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material, and depositing a conductive metal within the via and trench.

20. The method of claim 19 wherein the conductive metal is deposited on the integrated circuit chip outside of the via and the trench and the method further including the steps of planarizing the integrated circuit chip, and removing said excess conductive metal, the metallic mask layer and the barrier mask film.